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Voltage regulation in a power inverter using a quasi-sliding control technique

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Abstract
This paper shows the behavior of a three-phase power converter with resistive load using a quasi-sliding and a chaos control techniques for output voltage regulation. Controller is designed using Zero Average Dynamic (ZAD) and Fixed Point Inducting Control (FPIC) techniques. Designs have been tested in a Rapid Control Prototyping (RCP) system based on Digital Signal Processing (DSP) for dSPACE platform. Bifurcation diagrams show the robustness of the system. Chaos detection is a signal processing method in the time domain, and has power quality phenomena detection applications. Results show that the phase voltage in the load has sinusoidal performance when it is controlled with these techniques. When delay effects are considered, experimental and numerical results match in both of stable and transition to chaos zones.

Keywords: Power measurement, Power quality, Power electronics, Complexity theory, Chaos, Power Inverter.

Regulación de tensión en un inversor de potencia usando técnica de control cuasi deslizante

Resumen
Este documento presenta el desempeño de un inversor de potencia con carga resistiva usando una técnica de control cuasi deslizante y una técnica de control de caos para la regulación de la tensión de salida. El controlador se diseño usando técnicas de Dinámica de Promedio Cero (ZAD) y Punto Fijo de Control de Inducción (FPIC). Los diseños han sido probados en un sistema de Prototipado Rápido de Control (RCP) basado en un Procesador Digital de Señales (DSP) para la plataforma dSPACE. Los diagramas de bifurcaciones muestran la solides del sistema. La detección de caos se realiza por un método de procesamiento de señales en el dominio del tiempo, y tiene aplicaciones en detección de fenómenos de calidad de la potencia. Los resultados muestran que la tensión de fase de la carga tiene desempeño sinusoidal cuando se controla con las técnicas mencionadas. Cuando se consideran los efectos de retraso, los resultados simulados y experimentales coinciden en ambos casos en zonas estables y de transición a caos.

Palabras clave: Medida de potencia, Calidad de la Potencia, Electrónica de Potencia, Teoría Compleja, Caos, Inversor de Potencia.

1. Introduction

The study of variable structure systems uses bifurcation theory in order to determine the conditions in parameter values which generate stability changes, periodicity and chaotic dynamics in the system, and which allow us to define safe and stable operation zones. Knowledge of these operation ranges let us avoid the presence of non-desired phenomena such as auto-sustained oscillations, chaos, and evolution to other operation regimes, among others.

Control action required for three-phase loads is implemented usually by power electronic circuits based on switches. For this reason, controlled commuted system with three-phase-load (Resistive) becomes a variable structure system defined by non-smooth differential equations in which a complete theoretical framework does not exist yet allows its study [1] since its theoretical and numerical analysis represents an extremely difficult problem [3]. In this

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sense, non-smooth transitions occur when a cycle interacts with a boundary of discontinuity in the phase space in a non-generic way, causing periodic additions or sudden chaos transitions [4]. One of the most relevant aspects in the bifurcation analysis of non-smooth systems is the absence of the double periodic sequences that are observed in smooth systems [3]. Due to characteristic behavior of non-smooth systems, in many cases, it is not possible to apply analysis techniques for smooth systems without modifications or adequate adjustments [1].

Converters use power electronics for efficient transformation and rational use of electricity from the generation sources to its industrial and commercial use. It has been estimated that 90% of electrical energy is processed through power converters before the final use [5]. Power converters must provide a certain level of output voltage, either in task regulation or tracking, and they must be able to reject changes in load and primary supply voltage levels. A complete and detailed analysis of the operation and configuration of different power converters can be found in [6, 7]. One of the most desirable qualities in these devices is efficiency in the performance by using switching devices generating the desired output with low power consumption.

In general, the deterioration of power quality is due to non-stationary disturbances (voltage sags, voltage swells, impulses, among others) and also due to stationary disturbances (harmonic distortion, unbalance and flicker) [8-11]. In addition, the chaotic dynamics in the system under study generate non-periodic solution currents that are reflected on the source side, affecting other sensitive loads connected to the point of common coupling.

Controller designed in this work combines Zero Average Dynamics (ZAD) and Fixed Point Inducting Controller (FPIC) strategies, which have been reported in [18]. Design corresponds to a three-phase low power inverter (1500 W) with a three phase resistive load using a dSPACE platform for the control. Numerical and experimental bifurcations are obtained for the ZAD-FPIC-controller [22-24], by changing the parameter values. Obtained numerical and experimental bifurcation diagrams match. Development and application of the FPIC control technique are presented in [14,15,17,18]. This technique allows the stabilization of unstable orbits in a simple way.

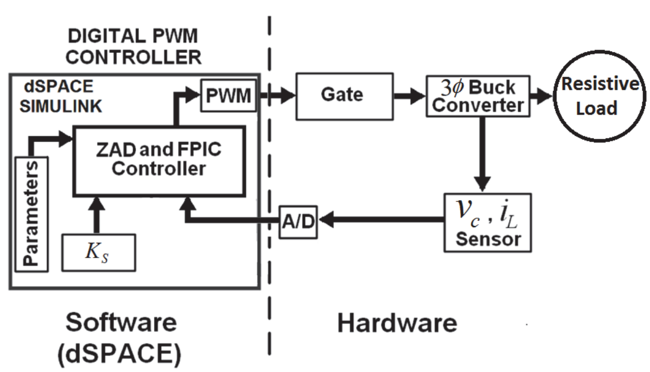


Figure 1. Block diagram of the proposed system
Source: The authors.

This paper is organized as follows. Section 2 describes the proposed system. Section 3 describes the mathematical model of the system. Section 4 describes the control techniques. Section 5 presents the obtained results, and finally, section 6 presents the conclusion.

2. Proposed system

Fig. 1 shows the block diagram of the system under study. This system is divided into two major subgroups, hardware and software. Hardware includes electrical circuits and electronic devices, and software includes signals acquisition and implementation of control techniques. The software is implemented in a dSPACE platform.

Hardware is composed of a Three–phase power converter with resistive load, which is rated to 1500W, 600 V DC and 20 A DC. For the measure of variables, v_c (capacitor voltage), a series resistance was used and for the measurement of i_L (inductor currents) HX10P/SP2 current sensors were used. Converter switches were driven by PWM outputs of the controller card; these signals are coupled via fast optocouplers (6N137).

Software is developed using the control and development card dSPACE DS1104, where ZAD and FPIC control techniques are implemented. The sampling rate for all variables is set to 4 kHz. The state variables v_c and i_L are stored at 12 bits; the duty cycle (d) is handled at 10 bits. Parameters of buck converter (C, L, r_S, r_L) and ZAD-FPIC–controller (K_S, N, F_S, R) are entered to the control block by the user, as constant parameters. K_S is the bifurcation parameter. For each sample the controller calculates in real time the duty cycle and the equivalent PWM signal to control the gate.

3. Mathematical model

Fig. 2 shows a basic diagram of the system. Buck power converter is used to feed the resistive load. Eq. (1) is obtained for the system model.

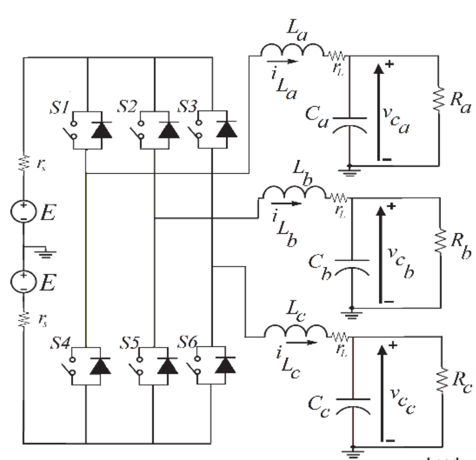


Figure 2. Electrical circuit for the 3-phase buck converter
Source: The authors.

$$\begin{bmatrix} \dot{v}_{c_a} \\ \dot{i}_{L_a} \\ \dot{v}_{c_b} \\ \dot{i}_{L_b} \\ \dot{v}_{c_c} \\ \dot{i}_{L_c} \end{bmatrix} = \begin{bmatrix} \frac{-1}{R_a C_a} & \frac{1}{C_a} & 0 & 0 & 0 & 0 \\ \frac{-1}{L_a} & \frac{-(r_s + r_{L_a})}{L_a} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{R_b C_b} & \frac{1}{C_b} & 0 & 0 \\ 0 & 0 & \frac{-1}{L_b} & \frac{-(r_s + r_{L_b})}{L_b} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{R_c C_c} & \frac{1}{C_c} \\ 0 & 0 & 0 & 0 & \frac{-1}{L_c} & \frac{-(r_s + r_{L_c})}{L_c} \end{bmatrix} \begin{bmatrix} v_{c_a} \\ i_{L_a} \\ v_{c_b} \\ i_{L_b} \\ v_{c_c} \\ i_{L_c} \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ \frac{E}{L_a} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & \frac{E}{L_b} & 0 \\ 0 & 0 & 0 \\ 0 & 0 & \frac{E}{L_c} \end{bmatrix} \begin{bmatrix} S_1 - S_4 \\ S_2 - S_5 \\ S_3 - S_6 \end{bmatrix} \tag{1}$$

With

$$S_4 = 1 - S_1$$
$$S_5 = 1 - S_2$$
$$S_6 = 1 - S_3$$

And

$$S_i \in \{0,1\}$$
$$for\ i = 1 \ldots 6$$

This equation can be expressed in a compact form as:

$$\dot{x} = Ax + BU \tag{2}$$

where the state variables are:

$v_{c_a} = x_1$, $i_{L_a} = x_2$, $v_{c_b} = x_3$, $i_{L_b} = x_4$, $v_{c_c} = x_5$, and $i_{L_c} = x_6$

A is a block diagonal matrix, so that the system consists of three uncoupled subsystems that may be treated independently. Fig. 3 shows the equivalent circuit per phase.

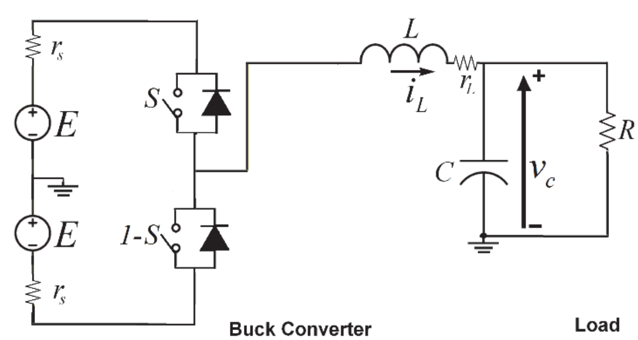


Figure 3. Electrical circuit for the buck converter (equivalent per phase)
Source: The authors.

3.1. Derivation of the discrete time iterative map of the converter

The inherent piecewise switched operation converters implies a multi-topological mode in which one particular circuit topology describes the system for a particular interval of time. The first step in the analysis of multi-topological circuit is to write down the state equations, which describes the individual switched circuits. For converters operating in the continuous conduction mode, two switched circuits can be identified. When the switch is ON, it is described by Eq. (3); when the switch is OFF, it is described by Eq. (4).

$$\begin{bmatrix} \dot{v}_c \\ \dot{i}_L \end{bmatrix} = \begin{bmatrix} \frac{-1}{RC} & \frac{1}{C} \\ \frac{-1}{L} & \frac{-(r_s + r_L)}{L} \end{bmatrix} \begin{bmatrix} v_c \\ i_L \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{E}{L} \end{bmatrix} \tag{3}$$

$$\begin{bmatrix} \dot{v}_c \\ \dot{i}_L \end{bmatrix} = \begin{bmatrix} \frac{-1}{RC} & \frac{1}{C} \\ \frac{-1}{L} & \frac{-(r_s + r_L)}{L} \end{bmatrix} \begin{bmatrix} v_c \\ i_L \end{bmatrix} + \begin{bmatrix} 0 \\ -\frac{E}{L} \end{bmatrix} \tag{4}$$

State variables are the capacitor voltage (v_c) and the inductor current (i_L). These equations can be expressed in a compact form as $\dot{x} = Ax + Bu$ with $x_1 = v_c$ and $x_2 = i_L$. E Denotes the converter power supply and depending on the control pulse voltage E or $-E$ is injected to the system through a PWM signal.

By considering continuous conduction mode (CCM) and according to centered PWM (Fig. 4), the control signal is defined as follows:

$$u = \begin{cases} +1 & \text{if} \quad kT \le t \le kT + dT/2 \\ -1 & \text{if} \quad kT + dT/2 < t < kT + T - dT/2 \\ +1 & \text{if} \quad kT + T - dT/2 < t < kT + T \end{cases} \tag{5}$$

Solution of the system (3) for $kT < t < (kT + dT/2)$ is given by:

$$x(t) = e^{A(t-kT)} x(kT) - A^{-1}[I - e^{A(t-kT)}]B$$

Solution of the system (4) for $(kT + dT/2) < t < (kT + T - dT/2)$ is given by:

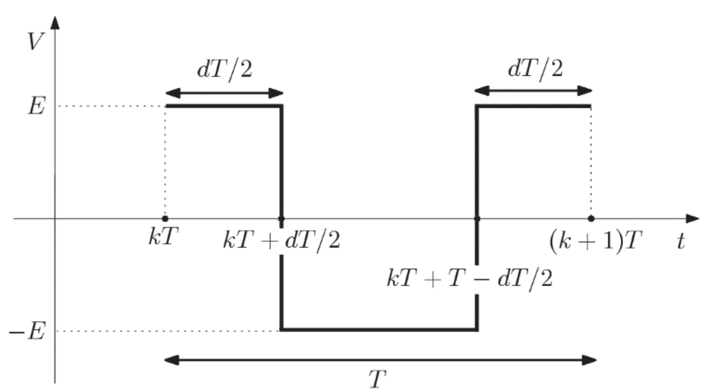


Figure 4. Centered PWM
Source: The authors.

$$x(t) = e^{A(t-(kT+dT/2))}x(kT + dT/2) + A^{-1}[I - e^{A(t-(kT+dT/2))}]B$$

where

$$x(kT + dT/2) = e^{A(dT/2)}x(kT) - A^{-1}[I - e^{A(dT/2)}]B$$

The solution of the system (3) for $(kT + T - dT/2) < t < (kT + T)$ is given by:

$$x(t) = e^{A(t-(kT+T-dT/2))}x(kT + T - dT/2) - A^{-1}[I - e^{A(t-(kT+T-dT/2))}]B$$

where

$$x(kT + T - dT/2) = e^{A(T-dT)}x(kT + dT/2) + A^{-1}[I - e^{A(T-dT)}]B$$

General solution of the system for $kT < t < (kT + T)$ is given by:

$$x((k+1)T) = e^{AT}x(kT) + [2e^{A(dT/2)} - 2e^{A(T-dT/2)} + e^{AT} - I]A^{-1}B \tag{6}$$

where k represents the k^{th} iteration, T is the sampling period and d is the duty cycle

Eq. (6) is the discrete-time state equation for the buck converter. In much of the literature, the terms iterative map, iterative function and Poincaré map have been used synonymically with discrete-time state equation.

4. Control strategies

The control strategies presented in this section are developed for the per phase equivalent circuit. So for the three phase system the control must be applied for each phase independently, taking into account that the reference voltage will be phase shifted according to the corresponding circuit phase.

4.1. Derivation of the discrete time iterative map of the converter

As reported in [19-21], one of the possibilities for computing the duty cycle is to define a surface and to force it to be zero in each iteration. The surface per phase is defined as a piecewise-linear function as (Fig. 5) given by:

$$s_{pwl}(t) = \begin{cases} s_1 + (t - kT)\dot{s}_+ & \text{if} \quad kT \le t \le t_1 \\ s_2 + (t - kT + \dfrac{d_k}{2})\dot{s}_- & \text{if} \quad t_1 < t < t_2 \\ s_3 + (t - kT + T + \dfrac{d_k}{2})\dot{s}_+ & \text{if} \quad t_2 \le (k+1)T \end{cases} \tag{7}$$

where the variables are described in (8) with $k_s = Ks * \sqrt{LC}$ a positive constant.

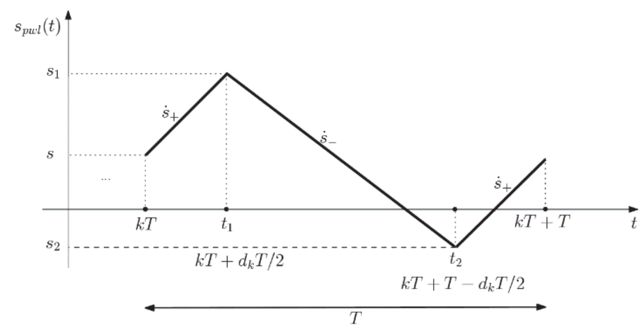


Figure 5. Surface to compute the duty cycle
Source: The authors.

$$\begin{aligned} \dot{s}_+ &= ((\dot{x}_1 - \dot{x}_{ref}) + k_s(\ddot{x}_1 - \ddot{x}_{ref}))\big|_{x=x(kT),u=1} \\ \dot{s}_- &= ((\dot{x}_1 - \dot{x}_{ref}) + k_s(\ddot{x}_1 - \ddot{x}_{ref}))\big|_{x=x(kT),u=-1} \\ s_1 &= ((x_1 - x_{ref}) + k_s(\dot{x}_1 - \dot{x}_{ref}))\big|_{x=x(kT),u=1} \\ s_2 &= \frac{d_k}{2}\dot{s}_1 + s_1 \\ s_3 &= s_1 + (T - d_k)\dot{s}_2 \\ t_1 &= kT + \frac{d_k}{2} \\ t_2 &= kT + (T - \frac{d_k}{2}) \\ t_3 &= (k+1)T \end{aligned} \tag{8}$$

The d_k satisfying zero average requirements is:

$$D_k = \frac{2s_1(x(kT)) + T\dot{s}_-(x(kT))}{\dot{s}_-(x(kT)) - \dot{s}_+(x(kT))} \tag{9}$$

From (3), (4) and (8) we obtain:

$$\begin{aligned} s_1(kT) &= (1 + ak_s)x_1(kT) + bk_sx_2(kT) - x_{1ref} - k_s\dot{x}_{1ref} \\ \dot{s}_+(kT) &= (a + a^2k_s + bck_s)x_1(kT) + (b + abk_s + bdk_s)x_2(kT) + bk_s\frac{E}{L} - \dot{x}_{1ref} - k_s\ddot{x}_{1ref} \\ \dot{s}_-(kT) &= (a + a^2k_s + bck_s)x_1(kT) + (b + abk_s + bdk_s)x_2(kT) - bk_s\frac{E}{L} - \dot{x}_{1ref} - k_s\ddot{x}_{1ref} \end{aligned} \tag{10}$$

with $a = -\dfrac{1}{RC}$, $b = \dfrac{1}{C}$, $c = -\dfrac{1}{L}$, $d = -\dfrac{(r_s + r_L)}{L}$

The duty cycle is given by (11).

$$d_k = \begin{cases} 1 & \text{if} \quad D_k > T \\ D_k / T & \text{if} \quad 0 \le D_k \le T \\ 0 & \text{if} \quad D_k < 0 \end{cases} \tag{11}$$

We have experimentally measured and noticed that there is a period of delay in the control action. In this case, the control action is taken from the data acquired in the past sampling time, and then we compute the duty cycle as:

$$d_k = \frac{2s_1(x((k-1)T)) + T\dot{s}_-(x((k-1)T))}{\dot{s}_-(x((k-1)T)) - \dot{s}_+(x((k-1)T))} \qquad (12)$$

To apply this technique we need to measure the states at the beginning of each sampling time. To do this, we carry out a synchronization between the measured signals and the start of the PWM. This synchronization is performed using a trigger signal obtained from the PWM, which gives the command to the ADC converter for reading v_C and i_L. On the other hand, we need to know the values of the parameters L, C, r_S, r_L. In this case, we suppose that these parameters will be constant and measurable. The load R may be unknown and in this case must be estimated.

Taking into account the strategies FPIC and ZAD [22, 23], the new duty cycle is calculated as follow:

$$d_{k-FPIC} = \frac{d_k(k) + N \cdot d^*}{N+1} \qquad (13)$$

Where $d_k(k)$ is calculated as (12) and d^* is the duty cycle calculated in steady state $(x_1(kT) = x_{1ref})$. From (9) we have:

$$d^* = D_k\big|_{x_1(kT)=x_{1ref}} = \frac{T}{2} + \frac{T[(1+\frac{r_s+r_L}{R})x_{1ref} + (\frac{L}{R} + (r_s+r_L)C)\dot{x}_{1ref} + LC\ddot{x}_{1ref}]}{2E} \qquad (14)$$

5. Numerical and experimental results

In this section numerical and experimental results are shown using K_S and N as bifurcation parameters, in addition the system behavior under frequency and voltage amplitude variations are illustrated graphically. Parameter values used in simulations and experiments are listed in Table 1; initially the reference voltage has a peak of 32V and 40Hz of frequency. For the simulation in SIMULINK model the fixed step size (fundamental sample time) in the configuration parameter was setting in $1/(4Fs)$.

Table 1
Units for Magnetic Properties

Parameter	Value
r_S: Internal resistance of the source	4 Ω
E: Input voltage	40 V
L: Inductance	1.6 mH
r_L: Internal resistance of the inductor	0.9 Ω
C: Capacitance	368 uF
N: FPIC control parameter	7
Fc: Switching frequency	4 kHz
Fs: Sampling frequency	4 kHz
$1T\_p$: 1 Delay time	0.25 ms
K_S: Control parameter	5

Source: The authors.

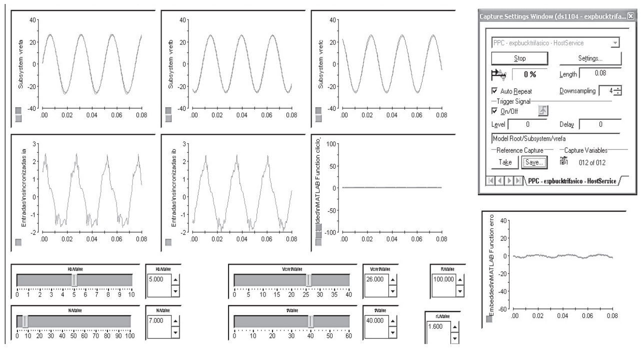


Figure 6. Periodic Solution for the three–phase converter with resistive load
Source: The authors.

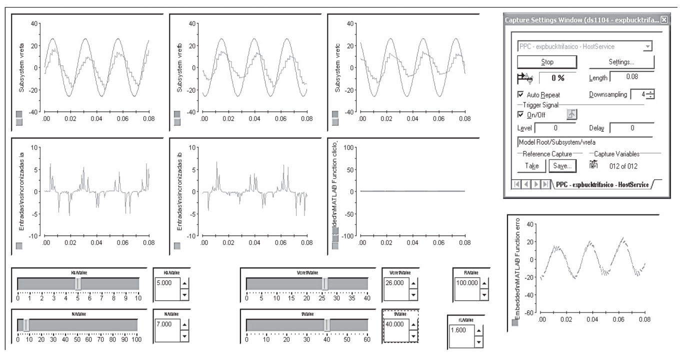


Figure 7. Chaotic Solution for the Three–phase converter with resistive load
Source: The authors.

Figs. 6 and 7 show the experimental behavior for the Three–phase power converter, using the same parameters and controller, but with different initial conditions. Reference Voltages for phases a, b, c (upper signals); phase voltages (v_a, v_b, v_c) and phase currents (i_a, i_b) (middle signals) are shown in these Figures.

In Fig. 6 the system exhibits a periodic solution and in Fig.7 a chaotic solution. This fact shows the coexistence of attractors or solutions in the system. When the solution is periodic, the controlled voltage follows the voltage reference by the control action unlike the chaotic solution, where the output voltage is lower than the reference and it has an irregular fashion, in this regime the phase currents have a higher peak. Sometimes the system toggles between two solutions while it is running, this happens when the solution is near to the border of two regions of attraction.

Results obtained in simulation and experiments for periodic solutions are shown in Fig. 8. The simulation was executed taking into account a 3T (0,75ms) delay in the duty cycle application. Under this condition simulation and experimental results match. Controlled voltage v_C follows reference voltage for all phases with a maximum error of 2V.

Fig. 9 shows the bifurcation diagrams for the output error and duty cycle of controlled system with K_S and N like bifurcation parameters, obtained via model simulation using Simulink of Matlab. For $K_S = 1,5$ with $N = 2$ and $N = 1,5$ with $K_S = 3$ the system presents a qualitative behavior change. Before $K_S = 1,5$ and $N = 1,5$ the system is in chaotic regime

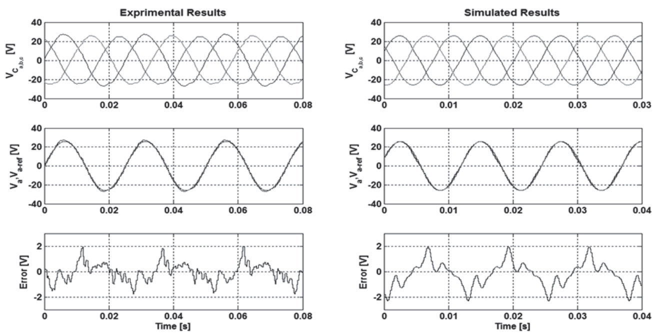
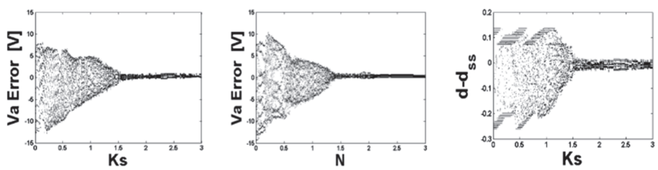


Figure 8. Experimental and simulation results for Three-phase converter with resistive load
Source: The authors.



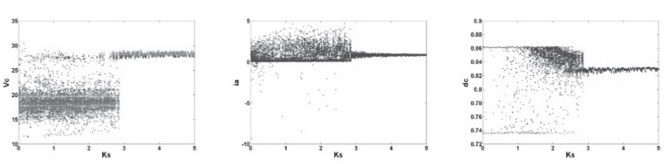
(a) Bifurcation Diagram with $N = 2$ (b) Bifurcation Diagram with $Ks = 3$ (c) Bifurcation Diagram with $N = 2$

Figure 9. Error in voltage, with *Ks* and N like bifurcation parameters, and error in duty cycle for phase a resulting from the model simulation using Simulink of Matlab of Three– phase converter with resistive load
Source: The authors.

and after it is in stable regime. For constructing these diagrams, the simulation was running for 3 periods of reference voltage and the last 15 samples of output error are taken with initial conditions equal to zero; also a delay in duty cycle application of 3T.

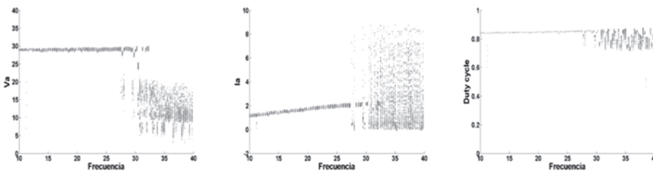
In the following the results of experiments are shown for buck power converter behavior when the voltage reference and voltage level vary.

Fig.10 shows the bifurcation diagrams for the output error and duty cycle of the controlled system with K_S and N as bifurcation parameters, obtained experimentally. For $K_S = 3$ the system presents a qualitative behavior change. Before $K_S = 3$ the system is in chaotic regime and after it is in stable regime. For constructing these diagrams, the experiment was run for 2 seconds for each value of K_S and samples were acquired every 50 milliseconds.



(a) v_c Bifurcation Diagram (b) i_a Bifurcation Diagram (c) Duty cycle Bifurcation Diagram

Figure 10. v_a voltage, i_a current and duty cycle experimental bifurcation diagrams with K_S like bifurcation parameter of three phasic converter with resistive load
Source: The authors.



(a) v_a Bifurcation Diagram (b) i_a Bifurcation Diagram (c) Duty cycle Bifurcation Diagram

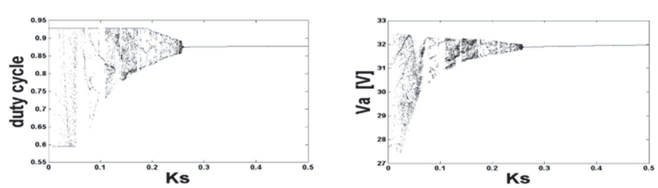
Figure 11. *Vc* voltage, ia current and duty cycle experimental bifurcation diagrams with f like bifurcation parameter of three phasic converter with resistive load
Source: The authors.

Fig. 11 shows the bifurcation diagrams for the i_a current, v_a voltage and duty cycle of controlled system with f (frequency of voltage reference) like bifurcation parameter, obtained experimentally. For $f \approx 27Hz$ the system presents a qualitative behavior change. After $f = 27Hz$ the system is in chaotic regime before its stable regime. For constructing these diagrams, the experiment was run for 2 seconds for each value of f and samples were acquired every 50 milliseconds. The phenomenon shown in Fig. 11 is caused by saturation of the inductor core in the *LC* filter; due to the fact that the core saturation and magnetic hysteresis not were simulated these phenomena are not present in simulations.

Fig. 12(a) shows the bifurcation diagram of duty cycle and Fig. 12(b) shows the bifurcation diagram of v_a for the Poincare map (6), both of which are numerical. Bifurcation diagrams were constructed taking the last 30 samples, each one for every period of reference voltage for phase *a* from the model (6) simulation using Matlab, while the system was running during 35 periods. The simulation was executed taking into account a single period (1T) of delay in the duty cycle application. In these Figures various regimes of operation can be appreciated: periodic windows, Chaos and periodic solutions.

Fig. 13 shows the bifurcation diagram when 3T of delay is considered. Bifurcation diagrams are quite different for different delay.

Before analysis shows the effects of the delay time in the signal control applied to the power converter. Many complex phenomena arise as shown in Figs. 13(e) and 13(f) some of these are not smooth bifurcations, double period bifurcations, chaos and 1-periodic orbits.



(a) Bifurcation Diagram of duty cycle for the Poincare map 4.6 (b) Bifurcation Diagram of v_a error for the Poincare map 4.6

Figure 12. Bifurcation Diagram with *Ks* like bifurcation parameters, taking one sample each period of the reference voltage for phase a during 30 periods considering a T delay
Source: The authors.

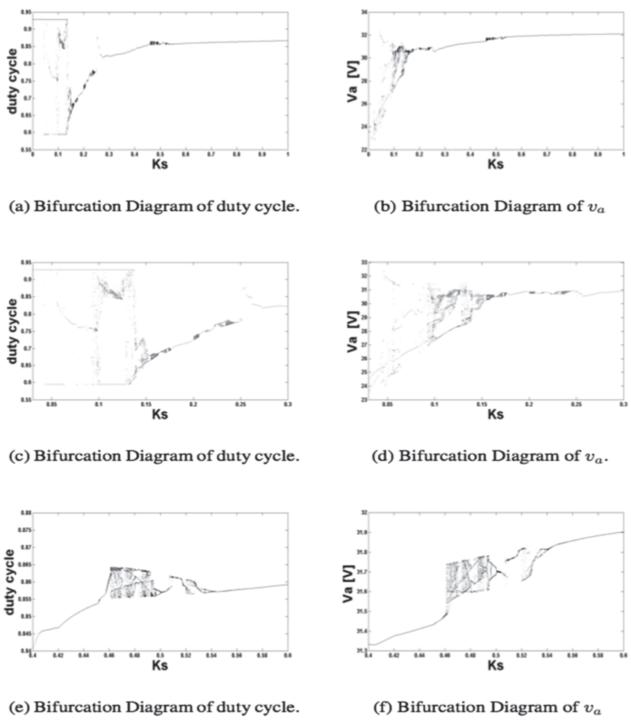


Figure 13. Bifurcation Diagram with *Ks* like bifurcation parameters, Taking a sample each 30 periods of the reference voltage for phase a considering a 3T delay, for the Poincare map 4.6 [
Source: The authors.

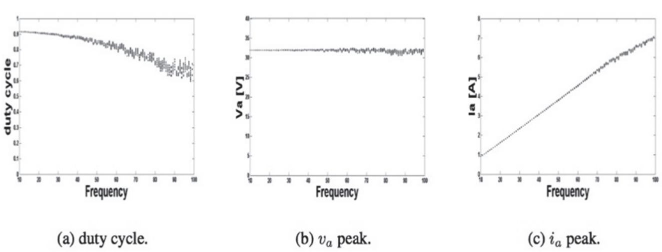


Figure 14. Results for Poincare map 4.6 simulation, Taking a sample on each one of last 10 periods of the reference voltage for phase a and ia considering a 3T delay, varying frequency in the reference voltage
Source: The authors.

In order to analyze the effect of the variation of frequency and voltage level in the reference voltage, a simulation was carried out.

Results obtained varying the frequency of reference voltage are shown in Fig. 14. The Figs. 14(a), 14(b), 14(c) show the behavior of duty cycle, peak voltage and peak current in C and L respectively when the frequency voltage reference is varied in the Poincare map simulation. The amplitude of the output voltage does not drop significantly with the variation of frequency, but the current peak has a linear growth with frequency, showing a predominant capacitive effect. In this case the delay does not have a significant impact.

5. Conclusion

Control strategy ZAD-FPIC was designed and applied to a three-phase buck converter with resistive load. For this system, simulations and experiments were performed. The stability of the closed loop system was analyzed using bifurcation diagrams; stability and transitions to chaos were observed. It was demonstrated in an experimental way, that the delay effects have high importance in the ZAD strategy. Simulations and experiments match when delay effects were included and improve the quality of the waves with ZAD control. Thus, in the chaos zone, a power quality deterioration by non-periodical current and voltage waveforms was observed, but, when the control is performed the non-periodicity is eliminated.

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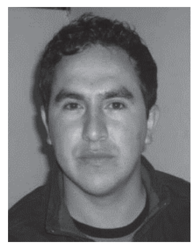

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