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# Grid-tied Multilevel Inverter with Phase-locked Loop Algorithm

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### Abstract

A multilevel inverter is an electronic device capable of changing direct current energy to alternant current energy with a voltage and frequency established by the user. They are ideal for connecting renewable energy sources to the AC grid, energy plants, and smart grids. The voltage must be balanced and synchronized with the electrical network for adequate performance. This paper shows the voltage synchronization between an inverter output voltage and the AC grid using a phaselocked loop based on an adaptive observer. The proposed algorithm can perform under grid uncertainties such as noise and generates a reference signal for the modulation used in the inverter. The algorithm is robust and computationally efficient and can be implemented through basic elements such as operational amplifiers, resistors, and capacitors, reducing its difficulty in executing it in a system.

**Keywords:** adaptive control; application of power electronics; Lyapunov methods; modelling.

## Inversor multinivel enlazado a la red eléctrica mediante un algoritmo de fijación de fase

#### Resumen

Un inversor multinivel es un dispositivo electrónico capaz de cambiar energía de corriente directa a energía de corriente alterna con voltaje y frecuencia establecidas por el usuario. Son ideales para conectar fuentes de energía renovables con la red eléctrica, plantas de energía y redes eléctricas inteligentes. Es necesario contar con el voltaje balanceado y sincronizado con la red para su correcto funcionamiento. Este artículo muestra la sincronización de la salida de voltaje del inversor con la red eléctrica utilizando un algoritmo de fijación de fase basado en un observador adaptable. El algoritmo propuesto puede funcionar ante incertidumbres de la red como el ruido y genera una señal de referencia para la modulación utilizada por el inversor. El algoritmo propuesto es robusto y computacionalmente eficiente, ya que puede ser implementado a través de elementos básicos como amplificadores operacionales, resistencias y capacitores, reduciendo la dificultad de ejecutarlo en un sistema.

**Palabras clave:** aplicación de electrónica de potencia; control adaptable; métodos de Lyapunov; modelado.

## Inversor multinível ligado à rede elétrica através de um algoritmo de fixação de fase

#### Resumo

Um inversor multinível é um dispositivo eletrônico capaz de alterar a potência de corrente contínua para potência de corrente alternada com tensão e frequência definidas pelo usuário. Eles são ideais para conectar fontes de energia renovável à rede elétrica, usinas de energia e redes inteligentes. É necessário ter uma tensão balanceada e sincronizada com a rede para seu correto funcionamento. Este artigo demonstra a sincronização da saída de tensão do inversor com a rede elétrica usando um algoritmo de fase baseado em observador adaptativo. O algoritmo proposto pode trabalhar diante de incertezas da rede como ruídos e gerar um sinal de referência para a modulação utilizada pelo inversor. O algoritmo proposto é robusto e computacionalmente eficiente, pois pode ser implementado por meio de elementos básicos como amplificadores operacionais, resistores e capacitores, reduzindo a dificuldade de executá-lo em um sistema.

**Palavras-chave:** aplicação em eletrônica de potência; controle adaptativo; métodos de Lyapunov; modelagem.

### I. INTRODUCTION

The interest in energy generation through renewable energy sources (such as solar energy and wind energy) has increased in recent years. Moreover, the benefits obtained by this form of generating energy are widely accepted and friendly to the environment [1-2]. The multilevel inverters are electronic devices that switch DC energy into AC energy and have been used to link the AC grid and renewable energy sources with the classic topologies (NPC, flying capacitor, and cascaded H-bridge) [3].

In addition to using multilevel inverters for conditioning the energy, it is necessary to have a control process to find the phase angle of the AC grid to synchronize the energies [4]. One way to achieve this is by using Phase-Locked Loop Algorithms (PLL) [5]. It consists of a control loop that generates an AC signal that is compared with a reference signal, obtaining information such as frequency, amplitude, and phase [6]. The first synchronization schemes were based on an open-loop estimation of the phase angle by detecting zero crosses [7]. Nevertheless, the presence of phenomena related to energy quality causes limitations for controllers of this type. To improve these negative aspects, phase tracking was implemented, and good results were obtained, and a harmonic oscillator controlled by voltage for compensating harmonic destabilization was added [8]. One of the most used methods is the fixed reference frame due to its positive performance [9-10]. However, its performance is adequate only with balanced systems. Therefore, other control schemes such as PI controllers and resonant controllers have been used for compensating the unbalances and harmonics on the grid.

The literature presents different PLL schemes for synchronizing multilevel inverters with the AC grid. For example, Rodriguez-Trujillo et al. [11] present the design, modeling, and implementation of a one-phase inverter connected with the mains by a PLL that generates a quadrature component with the voltage signal obtained from a delay. Rashed et al. [12] used a repetitive resonant controller for a grid-tied inverter with very distorted energy, where the proposed control obtains the angle, frequency, and amplitude of the grid fundamental. Moreover, Yue and Tolbert [13], a CHB of 11 levels synchronizes energy generated by photovoltaic solar panels with

the AC grid through a PLL with delay to generate a signal in quadrature. As a feature, it is necessary that the amplitude and phase are obtained quickly and precisely, independent of the technique used, even if the input signal is distorted. In general, there is an increase in the use of synchronization schemes, specifically PLLs for grid-tied multilevel inverters with renewable energy sources. This paper presents a grid-tied multilevel inverter with a PLL based on an adaptive observer. The PLL creates a reference signal that serves as a modulated signal, and then it is compared with triangular carriers signals of high frequency, which generates the pulse width modulation (PWM) for turning on and off the power semiconductor devices composing the inverter, thus, obtaining a robust control under uncertainties of the grid such as voltage sag, noise, and distorted signal.

### **II. METHODOLOGY**

## A. Multilevel Inverter and PLL Development

The topology selected is the one-phase five-level CHB, consisting of two H bridges, each one with four power semiconductor devices and a DC voltage source.

According to the literature, there are several techniques for obtaining a PWM for multilevel inverters. The PWM used in this paper is the high-frequency phase disposition PWM (PD-PWM) [14]. This PWM requires two carriers for each bridge which is compared in amplitude with a sinusoidal signal (modulated signal), as shown in Figure 1. In addition, Table 1 presents the output voltage obtained by turning on and off the power semiconductors of the inverter.



Fig. 1. High-frequency Phase Disposition PWM.

| $S_{11}$ | <i>S</i> <sub>12</sub> | <i>S</i> <sub>13</sub> | <i>S</i> <sub>14</sub> | $S_{21}$ | <i>S</i> <sub>22</sub> | <i>S</i> <sub>23</sub> | $S_{24}$ | $v_{CD}$   |
|----------|------------------------|------------------------|------------------------|----------|------------------------|------------------------|----------|------------|
| 0        | 0                      | 1                      | 1                      | 0        | 0                      | 1                      | 1        | 0          |
| 1        | 0                      | 0                      | 1                      | 0        | 0                      | 1                      | 1        | $v_{CD}$   |
| 1        | 0                      | 0                      | 1                      | 1        | 0                      | 0                      | 1        | $2v_{CD}$  |
| 0        | 1                      | 1                      | 0                      | 0        | 0                      | 1                      | 1        | $-v_{CD}$  |
| 0        | 1                      | 1                      | 0                      | 0        | 1                      | 1                      | 0        | $-2v_{CD}$ |

Table 1. Output voltage for the switches turning on and off.

The connection plan is depicted in Figure 2, where the signal obtained from the PLL serves as a modulated signal in the PD-PWM.



Fig. 2. System connection with the PLL.

For the PLL design, the input is considered a harmonic oscillator, and a state estimator with damping is built as a copy of the input, as shown in Equations (1) and (2). The damping is added to rebuild the phase angle. Subsequently, a clean version of the input is obtained, and the fundamental frequency is estimated.

$$\hat{\hat{v}}_{S} = -\hat{\theta}\hat{\psi} + \lambda \tilde{v}_{S} \qquad (1)$$

$$\hat{\psi} = \hat{v}_{S} \qquad (2)$$

Where  $\tilde{v}_s$  represents the error signal given by the difference between the input and the estimated,  $\hat{\psi}$  is an auxiliary signal in quadrature regarding the estimate of the input time derivative  $\hat{v}_s$ ,  $\hat{\theta}$  is the estimate of the phase angle of the input signal,  $\hat{v}_s$  is the estimate for the input signal, and  $\lambda$  is a positive design parameter for introducing the damping. An adaptive law is proposed for rebuilding  $\theta$ , following a Lyapunov approach as a storage energy function in Equation (3), taking the error signals over the trajectories and introducing  $\gamma$  as an adaptive gain.

$$V = \frac{\widetilde{v}_s^2}{2} + \frac{\widetilde{\psi}^2}{2} + \frac{\widetilde{\theta}^2}{2\gamma}$$
(3)

Where  $\tilde{v}_s = v_s - \hat{v}_s$ ,  $\tilde{\psi} = \psi - \hat{\psi}$ , and  $\tilde{\theta} = \theta - \hat{\theta}$ . The adaptive law  $\hat{\theta} = -\gamma \tilde{v}_s \hat{\psi}$  is proposed for making the derivative regarding the time, negative semi-definite as  $\dot{V} = -\lambda \tilde{v}_s^2$  [15].

## B. Adjustment Parameters of the PLL

A first approximation for adjusting the parameters  $\lambda$  and  $\gamma$  is considering that the system is operating in-balance conditions, that is,  $\psi = v_s$ , and assuming  $\hat{\psi} = \hat{\omega}_0 \omega_0$ , where  $\omega_0$  is the angular frequency of the input signal and  $\hat{\omega}_0$  is the estimate of the angular frequency. This yields the following system:

$$\hat{\boldsymbol{v}}_{S} = -\widehat{\boldsymbol{\theta}}\widehat{\boldsymbol{\psi}} + \lambda \widetilde{\boldsymbol{v}}_{S}$$
 (4)  
$$\hat{\boldsymbol{\psi}} = \widehat{\boldsymbol{v}}_{S}$$
 (5)

Next, a change of variables is proposed with  $\dot{x}_1 = v_S \hat{v}_S$ ,  $\dot{x}_2 = \omega_0 v_S$ , and  $\dot{x}_3 = \omega_0 - \hat{\omega}_0$ , obtaining the Equations (6), (7), and (8).

$$\dot{x}_1 = -x_3 x_2 - \lambda x_1$$
 (6)  
 $\dot{x}_2 = x_3 x_1 - \lambda x_2 + \lambda |v_S|^2$  (7)

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$$\dot{x}_3 = \frac{\gamma}{\omega_0^2} x_1 \tag{8}$$

Then, the gains adjustment is based on the desired bandwidth for a second-order system. For design purposes, it is considered a damping ratio of  $1/\sqrt{2}$ . The bandwidth (BW) must be less than  $2\omega_0$ , where  $\omega_0$  is the nominal value of the AC grid angular frequency. It is common in practice to select the bandwidth between 1/2 and 1/10 of that frequency. Under this consideration, the parameters can be adjusted with the Equations (9) and (10).

$$\lambda = \sqrt{2}\omega_{BW}$$
(9)  
$$\gamma = \left(\frac{\omega_0 \omega_{BW}}{|v_S|}\right)^2$$
(10)

#### **III. RESULTS**

Numerical results were obtained using Simulink of MATLAB, for the PLL based on the adaptive observer shown in Figure 3. Figure 4 shows the PLL capability to respond under abrupt change of signal. The change is from a 1V square signal to 1Vpp sinusoidal signal, both at 60Hz of frequency. The two signals (input and output) are spliced at the same graphic.



Fig. 3. PLL scheme implemented in Simulink.



Fig. 4. PLL response under change of signal.

Then, Figure 5 shows a zoom in the PLL response where the input is a square signal of 1.6Vpp at 60Hz. The PLL recovery time is around 0.00004 seconds.



Fig. 5. PLL zoom response where the input is a square signal.

Next, Figure 6 presents the phase portrait for the input signal versus the output signal, where the input is a sinusoidal signal. This evidences the similarity between signals.



Fig. 6. PLL phase portrait.

The PLL creates a reference signal obtained from the AC grid, and this signal serves as a modulated signal in the phase disposition PWM. This scheme is simulated to obtain the response shown in Figure 7.



Fig. 7. AC grid voltage and inverter voltage synchronization.

The prototype shown in Figure 8 was built for the experimental test having a 15kW inverter with the PLL and the modulation implemented through operational amplifiers [16]. The red rectangle shows the IGBTs, and this represents the power stage. The yellow square exhibits the high-frequency phase disposition PWM. The blue square is the PLL, and finally, the green rectangle is the signal conditioning (optocouplers, drivers, dead time).



Fig. 8. Grid-tied inverter prototype.

To corroborate the numerical results obtained for the PLL in Simulink, the PLL implemented through operational amplifiers was probed under changes of signal, signal with noise, and the phase portrait. Figure 9 depicts the PLL response under signal change from 1V square signal to 1Vp sinusoidal signal at 60Hz. The input signal comes from a Rigol signal generator. The peaks over the signal are produced by noise in the oscilloscope tips.



Fig. 9. PLL experimental response under change of signal.

Revista Facultad de Ingeniería (Rev. Fac. Ing.) Vol. 31 (60), e13847. May-June 2022. Tunja-Boyacá, Colombia. L-ISSN: 0121-1129, e-ISSN: 2357-5328. DOI: <u>https://doi.org/10.19053/01211129.v31.n60.2022.13847</u> Then, Figure 10 shows the PLL phase portrait for a sinusoidal input signal.



Fig. 10. PLL experimental phase portrait.

Finally, the PLL is connected to the AC grid and its output to the phase disposition PWM. Figure 11 depicts the result for the voltage synchronization between the multilevel inverter output and the AC grid.



Fig. 11. Grid-tied experimental setup response.

### **IV. DISCUSSIONS AND CONCLUSIONS**

This article presented a grid-tied multilevel inverter with a PLL based on an adaptive observer. The design process considered the AC input signal as a harmonic oscillator, and a state estimator was proposed as a copy of the model,

which incorporated an adaptive law to reconstruct the angular frequency. Regardless of whether the signal is square, triangular, sinusoidal, etc., as long as the signal is periodical, the PLL can reproduce it and obtain a clean version of it.

The PLL does not need to detect zero crosses or delays; it has a fast response, and the model of the algorithm is based directly on the AC grid without a fixed reference frame for obtaining the angle.

The algorithm is computationally efficient and can be implemented through basic elements such as operational amplifiers, resistors, and capacitors, reducing its difficulty in executing it in a system. A conventional technique is used (PD-PWM) for achieving the synchronization to the AC grid. Numerical results and experimental results were consistent.

Future research could finish the prototype and connect it to renewable energy sources such as photovoltaic solar cells.

## **AUTHORS' CONTRIBUTION**

**Roberto Martínez-Montejano:** Investigation, Methodology, Witing-review & editing, Funding acquisition.

Osbaldo-Ulisses Álvarez-Maldonado: Investigation, Writing-original draft.

José-Jimmy Jaime-Rodrpiguez: Visualization.

Germánico González-Badillo: Formal analysis.

Isaac Campos-Cantón: Validation.

Misael-Francisco Martínez-Montejano: Conceptualization, Supervision.

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