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INVESTIGACIÓN

Comparative analysis of threshold voltage extraction techniques based in the MOSFET gm/ID characteristic

Comparación de las técnicas de extracción del voltaje de umbral basadas en la característica gm/ID del MOSFET

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Abstract

Context: In advanced ultralow-power devices, it is necessary to use the accuracy extraction procedures of the MOSFET threshold voltage to fully characterize the devices. These procedures are based in the measurement of the Tran-conductance efficiency (gm/ID) and its first derivative in function of the voltage gate source (d(gm/ID)/dVGS). In order to increase their independency respect to the non-zero drain source voltage (VDS ≠0) it is used a process to correct the error. Theoretically, VDS should be 0 V; however, the VDS is grater than 10 mV in the experimental setup in order to avoid electrical noise, but less than a certain maximum value for allowing the MOSFET operation in the linear region of the weak inversion.

Objective: To compare the extraction procedure proposed by (MC Schneider et al., 2006) and the method proposed by (Rudenko et al., 2011) with a generic, controlled and coherent test scenario.

Method: This paper proposes a test scenario based on the Advanced Compact MOSFET model (ACM) of a long channel MOSFET made in a standard 0.35 mm CMOS process, implemented numerically in MATLABâ. The concept of Power Error Correction (PEC) was used to compare the two processes numerically; it quantifies the sensitivity of the extraction process to the effect by the non-zero voltage value of the VDS in the experimental setup (i.e., NZ-DS effect).

Results: The error correction procedure proposed by (Siebel et al., 2012, Schneider et al., 2006) estimates the NZ-DS effect better than the procedure proposed by (Rudenko et al., 2011), considering the average, maximum and minimum PEC obtained for both extraction methodologies for a long channel MOSFET fabricated in a standard CMOS process of 0.35 µm, when the VDS is less than 50 mV.

Conclusions: The Vth extraction procedure proposed by (MC Schneider et al., 2006) is more robust than the method proposed by (Rudenko et al., 2011) regarding the NZ-DS effect.

Keywords: Threshold Voltage Extraction, MOSFET Modeling, Gm/ID transconductance efficiency.

Resumen

Contexto: En los dispositivos de ultrabaja potencia son necesarios procedimientos precisos de extracción de voltaje de umbral del MOSFET. Estos se basan en la medición de la eficiencia de la transconductancia (gm/ID) y su primera derivada respecto al voltaje puerta-fuente (d(gm/ID)/ dVGS). Para

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aumentar en algunas decenas de mV la precisión del voltaje de umbral extraído, se recurre a un proceso de corrección de errores que disminuye la influencia del voltaje dreno-fuente (VDS) que teóricamente debería ser 0 V. Típicamente, en el montaje experimental, el VDS es mayor a 10 mV con el fin de evitar el ruido eléctrico, pero menor a un cierto valor máximo con el fin de permitir que el MOSFET siempre opere en su región lineal.

Objetivo: Comparar el procedimiento de extracción propuesto por Schneider *et al*. (2006) y el método propuesto por Rudenko et al. (2011) con un escenario de prueba genérico, controlado y coherente.

Método: Se implementó un escenario de prueba en el *software Matlab*® para un MOSFET de canal largo fabricado en un proceso estándar CMOS de 0,35 mm, usando el modelo Advanced Compact MOSFET (ACM). Para comparar los dos procesos de extracción se tomó el concepto de potencia de corrección del error (PEC), el valor de este cuantifica la sensibilidad del proceso de extracción con respecto al valor no 0V del VDS usado experimentalmente (i.e., efecto NZ-DS).

Resultados: Considerando el promedio, el máximo y el mínimo PEC obtenido para ambas metodologías de extracción, el procedimiento de corrección de errores propuesto en Siebel, Schneider y Galup (2012) y Schneider *et al*. (2006) estima el efecto NZ-DS mejor que el procedimiento propuesto en Rudenko *et al*. (2011) para un MOSFET de canal largo fabricado en un proceso estándar CMOS de 0,35 µm, cuando el VDS es inferior a 50 mV.

Conclusiones: El procedimiento de extracción de Vth propuesto por Schneider *et al*. (2006) es más robusto que el sugerido en Rudenko *et al*. (2011) con respecto al efecto NZ-DS.

Palabras clave: extracción del voltaje de umbral, modelamiento de MOSFET, eficiencia transconductancia Gm/ID.

INTRODUCTION

Power consumption awareness began in the nineties. Nowadays, every circuit has to face the power consumption issue in both portable devices (e.g., for increasing the battery life) and high-end circuits (e.g., for avoiding packages and reliability issues). The advances in the solid-state devices had a direct impact in the efficiency and the cost of the electronic equipment (Sarmiento 2004); in particular, high-efficient systems such as inverters (Fajardo et al. 2014) and power supplies (Hernández et al. 2012) have been explored using high-frequency power MOSFET (i.e., Metal-Oxide-Semiconductor Field-Effect Transistor). Considering the micro-scale electronic systems, the power consumption has had a big reduction since the first integrate circuit; furthermore, the power reduction started with the invention of the complementary metal–oxide–semiconductor (CMOS) technology that allows the reduction of the static power consumption. The designing of integrate circuits using ultra-low power techniques, such as supply voltage reduction, sub threshold operation, and Biasing MOSFETs at very low current are not rare nowadays. Consequently, there have been dedicated proposed models for modeling the MOSFET in all its operation regions, including weak, moderate and strong inversion (Schneider et al. 2010).

The estimation of the MOSFET threshold voltage (Vth) is critical to model the complementary metal–oxide–semiconductor (CMOS) circuits, particularly on the design of ultra-low-power devices (Rudenko et al. 2011), (Siebel et al. 2012). The Vth is basically the gate source voltage (VGS) level necessary in the MOSFET to start working in Strong Inversion (SI). To identify a hard threshold in the drain current (ID) vs. gate source voltage (VGS) characteristic is difficult, because the continuous nature of the involved physical phenomena. Therefore, many researches have proposed Vth definitions and extraction procedures (Siebel et al. 2012).

The extraction procedures generally use the ID vs. VGS characteristic of the MOSFET (Ortiz-Conde et al. 2002). Furthermore, most of them use only one regime of operation (i.e., ID–VG methods), the SI region or the Weak Inversion (WI) region in both its linear and saturation operation. However, the Vth extracted data using these approaches is inaccurate because the Vth occurs in the transition region between WI and SI (Schneider et al. 2010).

Recently, new physic-based Vth definitions have been proposed because of the introduction of charge-based models (Schneider et al. 2010). In addition, accurate extraction methods based in the measurement of the transconductance efficiency (gm/ID) and the transconductance efficiency change (d(gm/ID)/dVG) have been proposed by (Siebel et al. 2012, Schneider et al. 2006). Parasitic effects (such as drain or source series resistances and channel mobility degradation) tend to have less influence in these extraction techniques. Furthermore, they are less sensitive to short channel effects such as velocity saturation. However, these charge-based definition and extraction methods can be used for finding the conventional Vth value used in the potential-based models. The charge-based definition of the Vth involves a physically impossible extraction setup because both the gm/ID and the d(gm/ID)/dVG characteristics must be measured with the MOSFET operating at zero drain source voltage (VDS=0). However, the MOSFET in the real setup operates in its linear region with a very low voltage for decreasing the parasitic effects, but it is high enough to sense the ID (Schneider et al. 2010). All of these techniques propose a correction methodology in order to reduce the non-zero drain-to-source (NZ-DS) effect present on the Vth extraction methods, but a direct comparison of these methodologies based in the reported results is too difficult or even impossible to do. Recently, (Fajardo et al. 2013) proposed the power error correction (PEC) of NZ-DS effect concept to analyze the error correction in these methodologies of Vth extraction.

The fundamental purpose of this paper is to compare the accuracy of the gm/ID method proposed by (Schneider et al. 2006) and the d(gm/ID)/dVG method proposed by (Rudenko et al. 2011), using the power error correction (PEC) concept proposed by (Fajardo et al. 2013). Additionally, this paper develops a comprehensible presentation of the NZ-DS effect using analytical models, and implements a generic, controlled and consistent test scenario in MATLAB® for a long channel MOSFET made in a 0.35 mm CMOS standard process using the Advanced Compact MOSFET (ACM) model.

METHODOLOGY

Advanced Compact MOSFET (ACM) Model.

The ACM model represents the device behavior in all regimes of operation using an analytical equation set (Schneider et al. 2006). The following are the ACM equations explored in this paper (Equations (1) to (5)).

$$ID = \mu \frac{W}{L}\left[\frac{\left(Q'^{\,2}_{IS} - Q'^{\,2}_{ID}\right)}{2C'_{ox}n} - \phi_T\left(Q'_{IS} - Q'_{ID}\right)\right] \quad (1)$$

$$V_P - VS(\mathrm{D}) = \phi_t\left[\frac{Q'_{IP} - Q'_{IS(D)}}{nC'_{ox}\phi_t} + \ln\left(\frac{Q'_{IS(D)}}{Q'_{IP}}\right)\right] \quad (2)$$

$$V_P = \phi_{sa} - 2\phi_F - \phi_t\left[1 + \ln\left(\frac{n}{n-1}\right)\right] \approx \frac{VG - V_{th}}{n} \quad (3)$$

$$\frac{gm}{ID} = \frac{1}{n\phi_T - \frac{\left(Q'_{IS} + Q'_{ID}\right)}{2C'_{ox}}} \quad (4)$$

$$\frac{d}{dVG}\left(\frac{gm}{ID}\right) = \frac{1}{2C'_{ox}}\left(n\phi_t - \frac{Q'_{IS} + Q'_{ID}}{2C'_{ox}}\right)^{-2}\left(\frac{Q'_{IS}}{n\phi_t - \frac{Q'_{IS}}{C'_{ox}}} + \frac{Q'_{ID}}{n\phi_t - \frac{Q'_{ID}}{C'_{ox}}}\right) \quad (5)$$

Where, μ is the mobility of the carriers in the semiconductor substrate, C'_{ox} is the oxide capacitance per unit area, L and W are the channel length and the channel width of the MOSFET respectively, Q'_{ID} is the drain inversion charge density, Q'_{IS} is the source inversion charge density, Q'_{IP} is the pinch-off charge density, V_P is the channel pinch-off voltage, ϕ_F is the Fermi potential, ϕ_{sa} is the surface potential, VS is the source bulk voltage, VD is the drain bulk voltage, VG is the gate bulk voltage, n is the slope factor, and ϕt is the thermal voltage given equation (6) as follows.

$$\phi_t = \frac{kT}{q} \tag{6}$$

Where q is the elemental electron charge, k is the Boltzmann constant, and T the absolute temperature. A script was implemented for solving the equations (1) to (5), assuming that the MOSFET was in non-saturated operation in the WI region. Furthermore, the test scenario considered a long channel NMOS transistor (W/L=32mm/3.2mm) at a temperature of 27°C, and the technological parameters of the standard 0.35 mm CMOS process (i.e., acceptor doping concentration NA= 6x1016 cm^{-3}, oxide thickness tox=7.8 nm, low field mobility m_0 = 0.36238 m^2/V.s, and flat band voltage VFB=0.8 V). (Schneider et al. 2010) presents an analytic expression for the equilibrium threshold voltage (Vth); this expression allows the Vth calculus from technological parameters, as shown in (7).

$$V_{th} = V_{FB} + 2\phi_f + \gamma\sqrt{2\phi_f} \tag{7}$$

Where, γ is the so-called body-effect factor.

Threshold voltage (Vth) definitions

The Vth concept is directly related to the physical phenomenon that prevails in the current flow when the MOSFET goes from WI to SI. The Vth in the surface potential based models (Tsividis et al. 1999) is the VGS that produces a surface potential equal to twice the Fermi potential ($\phi_s = 2\phi_F$). On the other hand, in the charge-based models (i.e., EKV, ACM), the Vth is the VG value associated to the threshold inversion charge density (Q'_{th}). Addicionally, both Vth values are related by the analytic expressions (Siebel et al. 2012) summarized in table 1.

The Vth extraction is generally based in the gm/ID extraction (Siebel et al. 2012, Schneider et al. 2006) in advanced ultra-low power applications. In order to understand this methodology we must discuss the gm/ID and the (d(gm/ID)/dVG) concepts using the charge-based model framework. The gm/ID is a quality factor of how much transconductance (gm) is produced for a given unit of bias current (Binkley 2007). The gm/ID in the bipolar transistor device is maintained at a constant high value over multiple tens of collector current. Unfortunately, the MOSFET device gm/ID is maximum in the WI region (always less than the gm/ID of the bipolar transistor), and drops significantly when operating in the SI region (Schneider et al. 2010). The gm/ID behavior (i.e., high for MI and low for SI and soft in the transition) allows defining directly the Vth from a specific inversion charge using the ACM model.

Table 1. Charge based definition of threshold voltage summary.

Notation	Vth Definition	Gm/ID RPD VDS=0	Value of qI VGS=Vth	Relative difference to classical definition $\phi_s = 2\phi_F$
Vthq1	$Q'_I = -nC'_{ox}\phi_t$	50 %	1	$\phi_t\left(1+n\ln\left(\frac{n}{n-1}\right)\right)$
Vthq0.5	$\max\left(-\frac{\partial}{\partial v_g}\left(\frac{g_m}{I_D}\right)\right)$	100/3 %	0.5	$\phi_t\left(1+n\left[\ln\left(\frac{n}{2(n-1)}\right)-0.5\right]\right)$

Source: own work, based on (Schneider et al. 2006).

Defining the normalized inversion charge (q_I) by equations (8) and (4), we expressed the gm/ID as a function of the normalized charges in the MOS channel in equation (9). Also, using equations (8) and (2) we found the VDS as a function of the channel charges in equation (10). The normalized gm/ID (gm/IDn) can be calculated using equation (11), this expression was found using equations (10) and (9), and assuming VDS=0 (i.e., MOS capacitor analysis $q_I = q_{ID} = q_{IS}$). As shown in figure 1(a), the gm/IDn characteristic is monolithical and without discontinuities. Therefore, the relative to the peak drop (RPD) can be used as a metric if we choose a RPD of 50% as the transition point between WI and SI, the related inversion charge would be q_I=1.

$$q_I = \frac{Q'_I}{Q'_{IP}} \quad ; \quad Q'_{IP} = -nC'_{ox}\phi_t \tag{8}$$

$$\frac{gm}{ID} = \frac{1}{n\phi_T\left(1+q_{IS}+q_{ID}\right)} \tag{9}$$

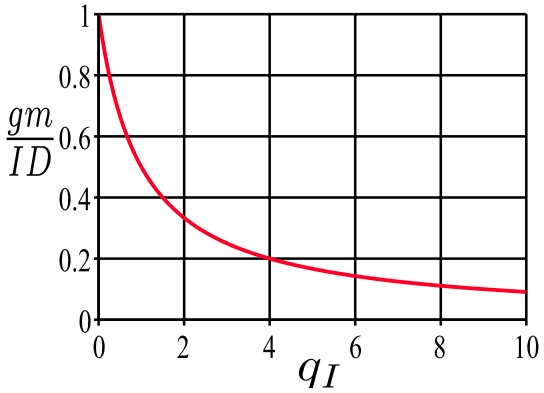
$$VDS = \phi_t\left[q_{IS} - q_{ID} + \ln\left(\frac{q_{IS}}{q_{ID}}\right)\right] \tag{10}$$

Where q_{IS} is the normalized source inversion charge, and q_{ID} is the normalized drain inversion charge. Another possible approach is to analyze the d(gm/ID)/dVG MOSFET characteristic: this characteristic may be interpreted like the d(gm/ID)/dVG for a given gate voltage change. The d(gm/ID)/dVG and its normalized value (d(gm/ID)/dVG) were found as a function of the normalized channel charges, following a similar procedure to the gm/ID characteristic. These are given by equations (12) and (13).

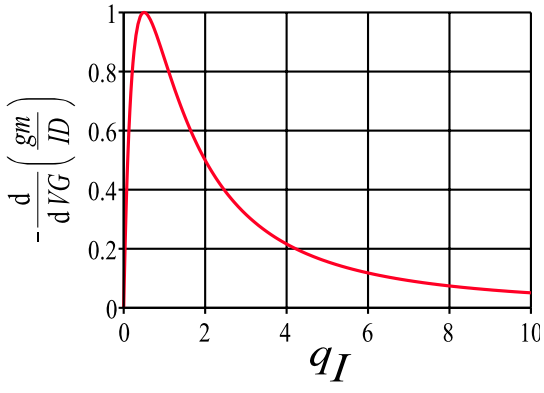
$$\left(\frac{gm}{ID}\right)_{nor} = \frac{gm}{ID}\left(\left(\frac{gm}{ID}\right)_{\max}\right)^{-1} = \frac{2}{2+q_{ID}+q_{IS}} = \frac{2}{2+2q_I} \tag{11}$$

$$-\frac{d}{dVG}\left(\frac{gm}{ID}\right) = \frac{1}{\left(n\phi_t\right)^2}\frac{\left(\frac{q_{IS}}{1+q_{IS}}+\frac{q_{ID}}{1+q_{ID}}\right)}{\left(2+q_{IS}+q_{ID}\right)^2} = \frac{2}{\left(n\phi_t\right)^2}\frac{\left(\frac{q_I}{1+q_I}\right)}{\left(2+2q_I\right)^2} \tag{12}$$

$$\left(-\frac{d}{dVG}\left(\frac{gm}{ID}\right)\right)_{nor} = \frac{d}{dVG}\left(\frac{gm}{ID}\right)\left(\frac{d}{dVG}\left(\frac{gm}{ID}\right)_{\max}\right)^{-1} = \frac{27}{4}\frac{q_I}{\left(1+q_I\right)^3} \tag{13}$$



a) gm/IDn vs q_I.



b) d(gm/ID)/dVGn vs. q_I

Figure 1. Transconductance MOSFET Characteristics**.**

Source: own work.

The gm/IDn and the d(gm/ID)/dVG are plotted in figure 1. As shown in figure 1(b), d(gm/ID)/dVGn has a maximum value between WI and SI (i.e., high and low values of q_i); therefore, this maximum is chosen as a threshold between WI and SI operation. On the other hand, gm/IDn (figure 1(a)) does not have any particular characteristic in the transition.

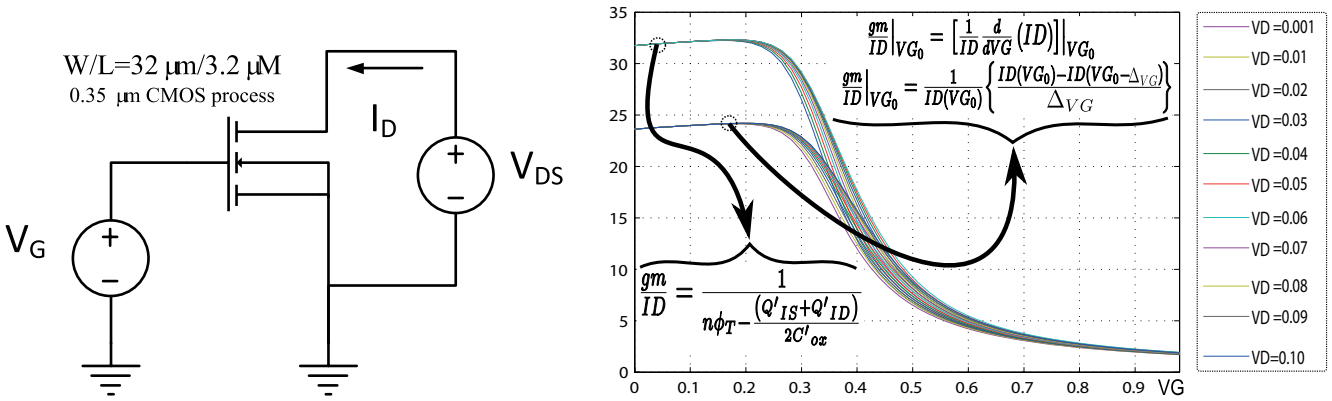
The common charge-based definition of Vth is $q_{Ith}=q_{Ith0.5}=0.5$ or $q_{Ith}=q_{Ith1}=1$. If we use the q_{Ith1} definition, the Vth is the voltage that produces the same drift and diffusion components of the drain current. On the contrary, if $q_{Ith0.5}$ is used for defining the Vth, it represents the voltage that produces the maximum value of the d(gm/ID)/dVG characteristic. The table 1 shows the Vth definitions, the used notation, the gm/ID RPD, the value of the q_i at Vth, and the voltage difference between the classical and the charge Vth definitions.

Transconductance efficiency (gm/ID) methods used for Vth extraction

Some error source in gm/ID and d(gm/ID)/dVG extraction process

The test setup used for the Vth extraction process (applying the gm/ID methods) is shown in figure 2(a). The VDS was replaced from 10mV to 50mV for any VDS value the gm/ID, and the d(gm/ID)/dVG characteristics were extracted as functions of the gate voltage. Additionally to the usual error involved in any empirical measurement, the error introduced by the numerical derivatives calculus of the gm/ID, the d(gm/ID)/dVG characteristics, and the NZ-DS effect must be considered in this experimental setup. To show error influence, some normalized gm/ID curve samples (for several ID values) were calculated using the charge based expressions of the ACM model (equations (1) to (5)); then these curve samples were evaluated using the numerically derivatives of the correspondent drain current samples. The resulting curves were plotted in figure 2(b) where it is possible to see the impact of the numerical error especially for low values of the gate voltage (low measured current).

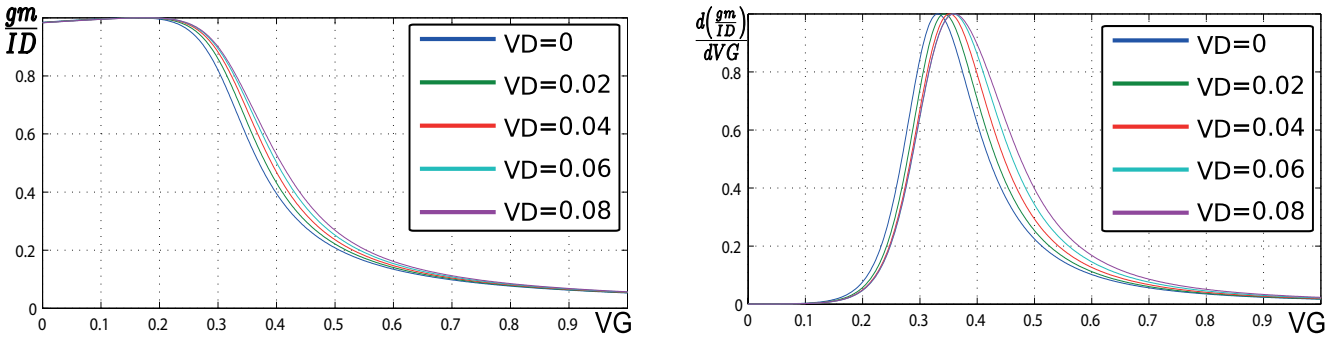
This work calculates the gm/ID and d(gm/ID)/dVG characteristics using the charge-based expressions which are the equations (4) and (5), so the error generated by the numerical calculus of these characteristics is not present. Furthermore, this controlled environment permits to evaluate in an easy way the PEC for the NZ-DS effect on the accuracy Vth extraction for advanced ultra-low power devices proposed by (Siebel et al. 2012, Schneider et al. 2006) because it is the only error source present in the extraction methodology.



a) Circuit topology for measures. b) Extracted by derivative calculus.

Figure 2. gm/ID characteristic.

Source: own work



a) gm/ID vs. VG. b) d(gm/ID)/d VG vs. VG.

Figure 3. Some normalized characteristic results.

Source: own work

In order to analyze the NZ-DS effect, figure 3 presents the gm/ID and d(gm/ID)/dVG characteristics calculated with the charge-based expressions. In figure 3(a) it is clear that the NZ-DS effect is increased by the VDS growth, therefore the Vth extracted using the operational definition (RPD of 50% or 75%) increases too. Secondly, figure 3(b) makes it clear that the NZ-DS effect is the variation of the d(gm/ID)/dVG maximum point. In conclusion, the NZ-DS effect increases the extracted Vth; this effect must be corrected in order to have better accuracy of the extraction procedures in some mV.

The Vth extraction procedures based in the gm/ID characteristic.

When the VG=Vth and VS=0 (because our circuit topology $q_{IS}= q_{th}$), and using equation (8), we can rewrite equation (10) as equation (16).

$$VD = \phi_t \left[q_{I_{th}} - q_{ID} + \ln\left(\frac{q_{I_{th}}}{q_{ID}} \right) \right] \qquad (14)$$

Then, we found the gm/ID value related to the Vth charge condition as a function of the VD. Furthermore, we found the analytical expressions of the normalized gm/ID (i.e., gm/IDn) as a function of the VD using the common charge-based definitions of Vth (i.e., $q_{Ith}=q_{Ith0.5}=0.5$ and $q_{Ith}=q_{Ith1}=1$) and equations (11) and (14). These founded expressions are given by equations (15) and (16).

$$\left(\frac{gm}{ID} \right)_{nq0.5} = \frac{2}{2.5 + \left(W_0 \left\{ 0.5 \cdot \exp\left(\frac{\phi_t - 2 \cdot VD}{2\phi_t} \right) \right\} \right)^{-1}} \qquad (15)$$

$$\left(\frac{gm}{ID} \right)_{nq1} = \frac{2}{3 + exp\left(1 - \frac{VD}{\phi_t} - W_0 \left\{ \exp\left(1 - \frac{VD}{\phi_t} \right) \right\} \right)} \qquad (16)$$

Where the $gm/IDn_{q0.5}$ and gm/IDn_{q1} are the gm/IDn values related to the VGS (or VG) that creates a superficial inversion charge density of $q_{Ith1^*}Q'_{IP}$ and $q_{Ith0.5^*}Q'_{IP}$ respectively; $W_0\{*\}$ is the Lambert function (Corless et al. 1996). This expression can be simplified for very low values of VDS as $gm/IDn_{q0.5} = 2/3$ or $gm/IDn_{q1}=0.5$. Therefore, the extraction procedures consist of determining the gate voltage (i.e., $V_{thq0.5}$ or V_{thq1}) at which the gm/IDn vs. VGS characteristic is equal to 50% or 66.66%. Then it is necessary to correct the NZ-DS effect of the extracted value. (Siebel et al. 2012, Schneider et al. 2006) reports a closed expression for calculating the incremental error present in the gm/ID characteristic Δ(gm/ID), these errors for $q_{Ith0.5}$ and q_{Ith1} are given by equations (17) and (18).

We used the incremental error in the gm/IDn and then extract the Vth ($V_{thq0.5}$ or V_{thq1}) by simply determining the VGS at which the gm/IDn characteristics are equal to the ideal condition plus the incremental error (equation (19)).

Figure 4(a) shows the Δ(gm/ID) behavior for low values of VDS, and figure 5(a) illustrates all the extracting process. On the other hand, (Rudenko et al. 2011) proposes for $V_{thq0.5}$ an error correction based in the incremental error ΔVth, given by equation (20).

$$\Delta\left(\frac{g_m}{ID}\right)_{nq0.5} = \left(\frac{gm}{ID}\right)_{nq0.5} - \frac{2}{3} \qquad (17)$$

$$\Delta\left(\frac{g_m}{ID}\right)_{nq1} = \frac{2}{3+exp\left(1-\frac{VD}{\phi_t}-W_0\left\{\exp\left(1-\frac{VD}{\phi_t}\right)\right\}\right)} - 0.5 \qquad (18)$$

$$\left(g_m/ID\right)_{n_{q1(0.5)}} = \left(g_m/ID\right)_{n_{q1(0.5)},V_{DS}=0} + \Delta\left(g_m/ID\right)_{n_{q1(0.5)}} \qquad (19)$$

$$\Delta Vth = n\phi_t\left[\ln(0.5) + \ln\left(\sqrt{1+\frac{16}{1+\exp\left(-\frac{2}{3}\frac{V_D}{\phi_t}\right)}}-1\right) + 0.25\left(\sqrt{1+\frac{16}{1+\exp\left(-\frac{2}{3}\frac{V_D}{\phi_t}\right)}}-3\right)\right] \qquad (20)$$

Δvg is shown in figure 4 (b). The error less Vthq0.5 is equal to the ideal condition plus the incremental error (equation (21)).

$$V_{th0.5} = V_{th0.5,V_{DS}=0} + \Delta Vth \qquad (21)$$

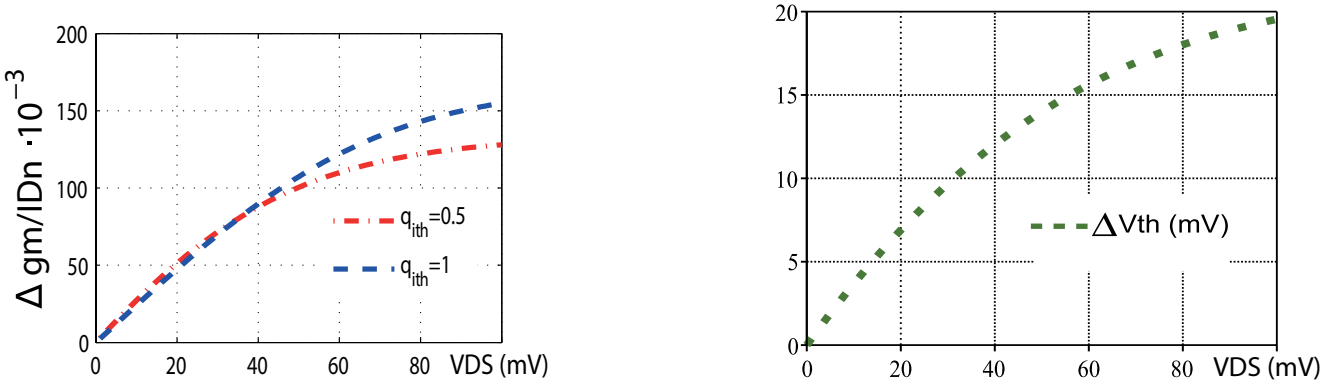
Where we extracted the $V_{thq0.5}$ from the gm/IDn characteristic (RPD 66.66%) or from d(gm/ID)/dVG characteristic (Vth=VGS where d(gm/ID)/dVG is maximum), then we estimate the error with equation (20) and determine the $V_{thq0.5}$ using equation (21). Figure 5(b) illustrates all the extracting processes for the d(gm/ID)/dVG characteristic.

Power Error Correction in Vth extraction gm/ID Methods

(Fajardo et al. 2013) defines the PEC with the following equation (22).

$$PEC = 100\cdot\left(1-\frac{E_c}{E_0}\right) \qquad (22)$$

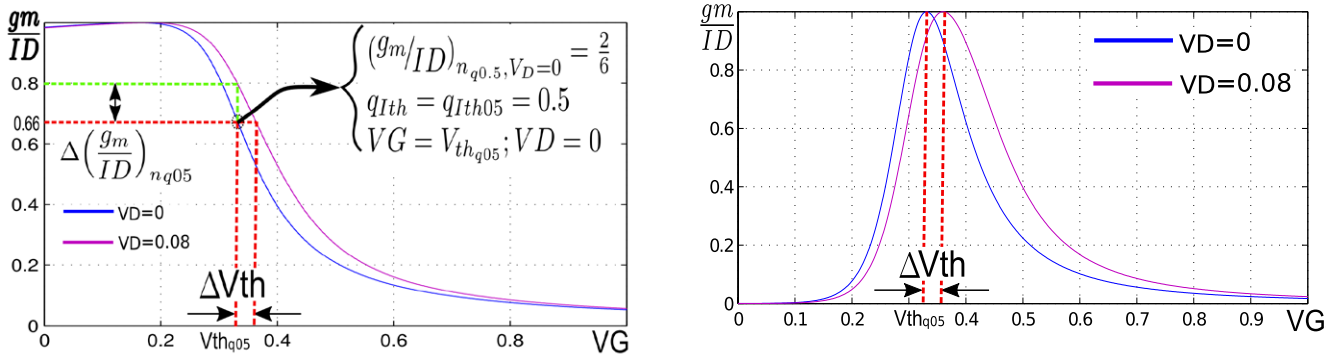
Where E_C is the error of the extracted Vth for a VDS sweep from 0 mV to V_{max} using the correction factor of the method, and E_0 is the mean of the extracted Vth for the same VDS sweep without using the correction factor. The V_{max} value is a technology value for a particular analyzed device; particularly for the long channel NMOS transistor studied in this paper, this value was set to 50 mV.



a) Δgm/ID b) ΔVth

Figure 4. NZ-DS effect correction factor

Source: own work



a) On the gm/ID characteristic. b) On the d(gm/ID)/d characteristic.

Figure 5. NZ-DS effect

Source: own work

RESULTS

Consistency Analysis of the simulation results and the extraction methods.

First, we extracted the Vth from the simulation data using the charge-based expressions (figure 6(a)). The extracted values were sumarized in equation (23).

$$v_{thq0.5} = 333.4\ mV \quad ; v_{thq1} = 370.2\ mV \qquad (23)$$

Where $v_{thq0.5}$ and v_{thq1} are the Vth extracted values using the charge-based definition $q_{Ith}=q_{Ith0.5}=0.5$ and $q_{Ith}=q_{Ith1}=1$, respectively. Second, we extracted the value of the slope factor (n) for these MOSFET operation points using the simulation data

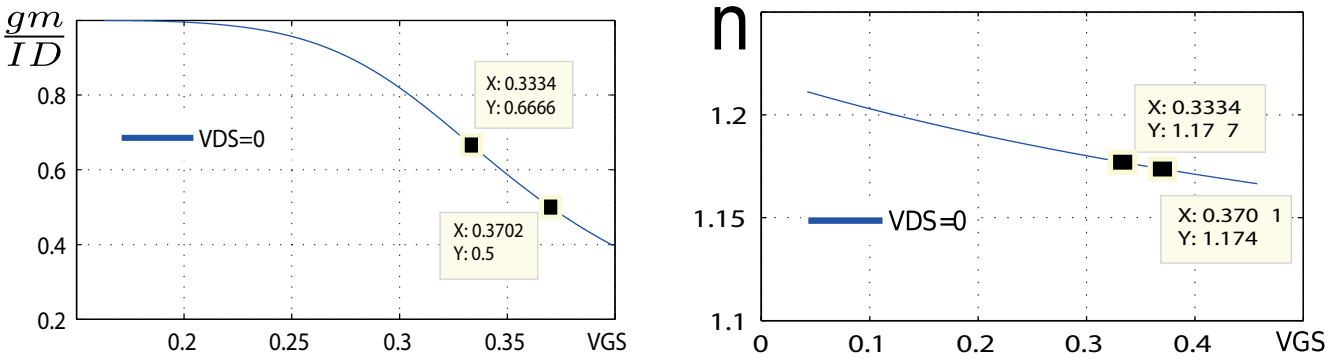
(figure 6(b)), and the extracted values were sumarized in equation (24).

$$n\left(v_{thq_{0.5}}\right)=1.177 \quad ; n\left(v_{thq_1}\right)=1.174 \tag{24}$$

We estimated the classical Vth (the Vth used in the potential-based models) of this process from the values in equations (23) and (24) and using the relationship beetween the classical definition and the charge-based definition of Vth, summarized in table 1. Equation (25) shows the results.

$$v_{th1} = 286.7\ mV \quad ; v_{th2} = 285.8\ mV \tag{25}$$

Where v_{th1} and v_{th2} are the estimated values of the classical Vth and were based on $q_{lth0.5}$ and q_{lth1} respectively.



a) Vth from gm/ID vs. VG with VDS=0. b) Slope Factor at the extracted Vth values.

Figure 6. Extraction parameters from the numerical simulation.

Source: own work

Finally, we calculated the Vth of this process using equation (7). The resulting value was 283.6 mV. As we expected, the extracted and calculated values of the Vth were almost the same (the error was less than 3mV); therefore, it is possible to affirm that the test scenario for a long channel MOSFET implemented in MATLAB® is consistent.

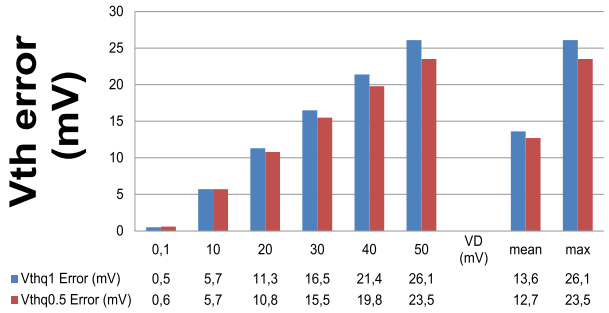
Vth Results using gm/ID method

Using the generic, controlled and consistent test scenario for the long channel MOSFET fabricated in a 0.35 mm CMOS standard process, we obtained from both gm/ID and d(gm/ID)/dVG the V_{thq} data with and without correction for a parametric sweep of the VDS from 0.1mV to 50mV. Figure 7 presents the Vth extracted from the charge-based expressions (with and without NZ-DS effect). The PEC was calculated for the analyzed methodologies using equation (22), and the results were summarized in figure 7. If we consider all the analyzed VDS range (100mV-50mV), the error correction procedure proposed by (Siebel et al. 2012, Schneider et al. 2006) estimates the NZ-DS effect better than the procedure proposed by (Rudenko et al. 2011) in the case of a long channel MOSFET fabricated in a 0.35 mm CMOS standard process, but in the range near the typical voltage used in an experimental setup (VDS=10mV-20mV) the PEC of both methodologies is similar.

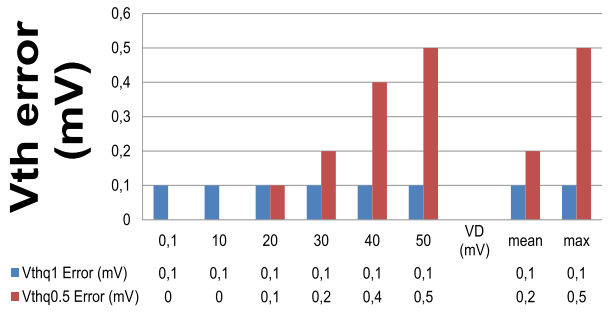
Comparative analysis of the PEC.

Figure 8 presents the mean, the maximum, and the minimum PEC achieved for each methodology in order to compare the two analyzed Vth extraction

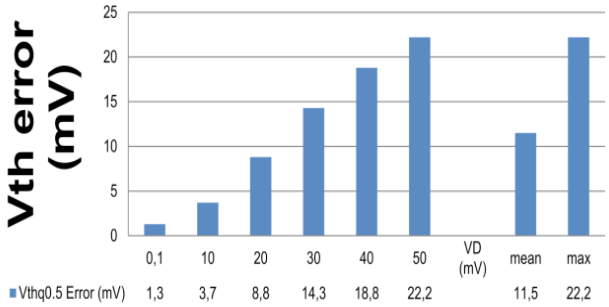
methodologies. Considering this figure, the error correction procedure proposed by (Siebel et al. 2012, Schneider et al. 2006) estimates the NZ-DS effect better than the procedure proposed by (Rudenko et al. 2011) for a long channel MOSFET fabricated in a 0.35 mm CMOS standard process when the VDS is less than 50mV. This methodology permits PEC always better than 80%; therefore, the correction procedure proposed by (Siebel et al. 2012, Schneider et al. 2006) is more robust and reliable than the procedure proposed by (Rudenko et al. 2011).



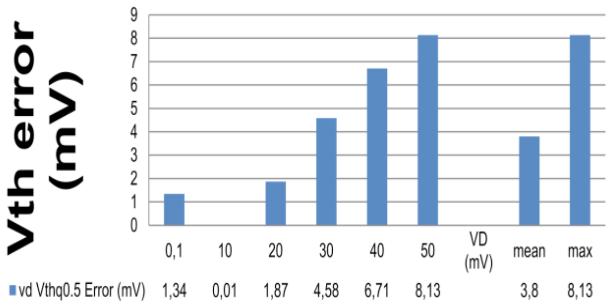
a) gm/ID w/o correction.



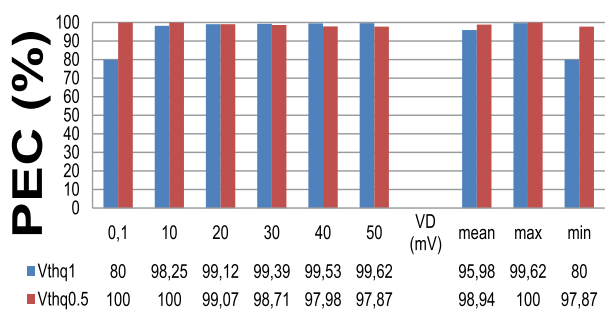
b) gm/ID with correction.



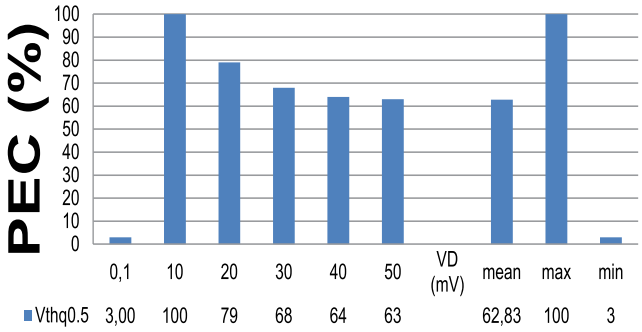
c) d(gm/ID)/dVG w/o correction.



d) d(gm/ID)/dVG with correction.



e) PEC results using gm/ID.



f) PEC results using d(gm/ID)/dVG.

Figure 7. Vth error using gm/ID and d(gm/ID)/dVG with and without NZ-DS correction.

Source: own work

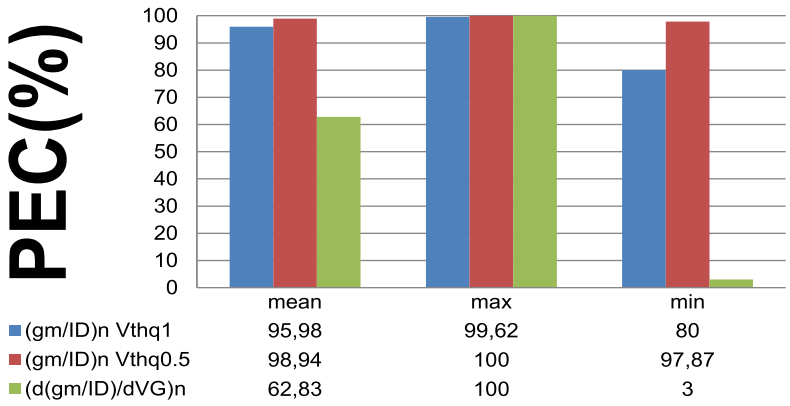


Figure 8. Comparative analysis of the PEC of NZ-DS effect correction

Source: own work

CONCLUSIONS

This paper compares the common extractions techniques proposed by (Rudenko et al. 2011, Siebel et al. 2012) in presence of non-zero drain source voltage (NZ-DS) effect, using the PEC concept proposed by (Fajardo et al. 2013) and a generic, controlled and consistent test scenario for a long channel MOSFET fabricated in a 0.35 mm CMOS standard process. In all the device operation on the linear region, the error correction procedure proposed by (Siebel et al. 2012, Schneider et al. 2006) estimates the NZ-DS effect better than the procedure proposed by (Rudenko et al. 2011), but in the typical voltage used in an experimental setup both methodologies are similar.

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